REMARKS

In accordance with the foregoing, claims 2 and 7 have been amended and claims 3 and 8 have been cancelled without prejudice or disclaimer. Claims 1, 2, 4, 5, 7, 11 and 12 are pending and under consideration. Claims 1, 11 and 12 are the independent claims. No new matter is presented in this Amendment.

REJECTIONS UNDER 35 U.S.C. §112:

Claims 2, 7 and 8 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicants note that claims 2 and 7 have been amended to correct the minor informality noted by the Examiner.

Accordingly, Applicants respectfully request that the rejection of claims 2 and 7 under 35 U.S.C. §112, second paragraph be withdrawn.

Regarding the rejection of claim 8, it is noted that claim 8 has been cancelled without prejudice or disclaimer. Accordingly, the rejection of claim 8 is moot.

REJECTIONS UNDER 35 U.S.C. §102:

Claims 1-3, 5, 7-8 and 11-12 are rejected under 35 U.S.C. §102(b) as being anticipated by Mitanaga et al. (U.S. Patent 5,923,997).

Applicants respectfully traverse this rejection for at least the following reason.

Regarding the rejection of independent claim 1, it is noted that claim 1 recites a display device with a polysilicon substrate, comprising: **a display region**; a driving region; **a first plurality of thin film transistors in the display region**; a second plurality of thin film transistors in the driving region; primary crystal grain boundaries in the polysilicon substrate in the display region and in the driving region; secondary crystal grain boundaries in the polysilicon substrate in the display region and in the driving region; **wherein** the **primary crystal grain boundaries** are **inclined** to a first direction of current flowing from source to drain of each of the first plurality

of thin film transistors **at an angle of -30° to 30°** and the secondary crystal grain boundaries are inclined to a second direction of current flowing from source to drain of each of the first plurality of thin film transistors, and wherein the primary crystal grain boundaries are inclined to the second direction of current flowing from source to drain of each of the second plurality of thin film transistors at an angle of 30° to 150° and the secondary crystal grain boundaries are inclined to the first direction of the current flowing from source to drain of each of the second plurality of thin film transistors.

The Office Action relies on Mitanaga for a teaching of a display region and a driving region and in particular relies on FIG. 2, items 111, 113 and column 13, line 11 through column 14, line 55.

However, a careful review of Mitanaga indicates that items 111, 113, 114 and 116 are not display or driving regions but simply n-type impurity regions and p-type impurity regions. Mitanaga discloses forming a region of a p-channel TFT (PTFT) and a region of an n-channel TFT (NTFT) (column 12, lines 5-9). The only reference Mitanaga makes of a display is at column 15, lines 33-36, but Mitanaga does not teach how the display portion is related to the impurity regions.

The Office Action further states that Mitanaga teaches a first plurality of TFTs in the display region and a second plurality of TFTs in the driving region and relies once again on the PTFT and NTFT for such teachings.

However, Mitanaga does not disclose where the TFTs are located in relation to a display region or a driving region, particularly since Mitanaga does not disclose a driving region.

Finally, the Office Action indicates that Mitanaga teaches that the **primary crystal grain boundaries** are **inclined to** a **first direction** of current flowing from source to drain of each of the first plurality of thin film transistors at an angle of -30° to 30° **and** the **secondary crystal grain boundaries** are **inclined to a second direction** of current flowing from source to drain **of** each of the **first plurality of thin film transistors**.

However, Mitanaga discloses that in an LCD device, the TFTs prepared in the **display portion** for switching each pixel need not to have a so high mobility but it is necessary to minimize a leak current, i.e., the current when the TFT is in its off state. For this reason, the direction of the source and drain regions are so designed in such a manner that the **current crosses grain boundaries** formed within the channel regions of the TFT. Therefore, unlike

previous embodiments, it is so designed that the direction in which the **crystallization proceeds** is **perpendicular to the current flow** direction in the TFT (FIG. 5C, column 15, lines 33-44). In other words, Mitanaga teaches that the primary crystal grain boundaries are formed in a direction which is perpendicular to the direction of the current flowing from the source to the drain.

Contrary to Mitanaga, independent claim 1 recites that the primary crystal grain boundaries are inclined to a first direction of current flowing from source to drain of each of the first plurality of thin film transistors at an angle of -30° to 30°. In other words, the primary crystal grain boundaries are substantially parallel to the direction of the current flowing from the source to the drain, and not perpendicular as taught by Mitanaga.

Accordingly, Applicants respectfully assert that the rejection of claim 1 under 35 U.S.C. § 102(b) should be withdrawn because Mitanaga fails to teach or suggest each feature of independent claim 1.

Furthermore, Applicants respectfully assert that the rejection of dependent claims 2, 5 and 7 under 35 U.S.C. §102(b) should be withdrawn at least because of their dependence from claim 1 and the reasons set forth above, and because the dependent claims include additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claims 2, 5 and 7 also distinguish over the prior art.

Regarding the rejection of dependent claims 3 and 8, it is noted that these claims have been cancelled without prejudice or disclaimer. Accordingly, the rejection of claims 3 and 8 is moot.

Regarding the rejection of independent claim 11, it is noted that claim 11 recites a display device with a polysilicon substrate comprising: a driving region; a plurality of **thin film transistors in the driving region**; primary crystal grain boundaries in the polysilicon substrate in the driving region; and secondary crystal grain boundaries in the polysilicon substrate in the driving region; wherein the **primary crystal grain boundaries** are **inclined** to a direction of current flowing from source to drain of each of the plurality of thin film transistors **at an angle of 30° to 150°** and the secondary crystal grain boundaries are substantially parallel to the current flowing from the source to the drain.

As noted above, Mitanaga discloses that in an LCD device, the TFTs prepared in the

display portion for switching each pixel need not to have a so high mobility but it is necessary to minimize a leak current, i.e., the current when the TFT is in its off state. For this reason, the direction of the source and drain regions are so designed in such a manner that the current crosses grain boundaries formed within the channel regions of the TFT. Therefore, unlike previous embodiments, it is so designed that the direction in which the crystallization proceeds is perpendicular to the current flow direction in the TFT (FIG. 5C, column 15, lines 33-44). In other words, Mitanaga only discloses the orientation of the primary crystal grain boundaries in a display portion but is silent with respect to the orientation of either primary or secondary grain boundaries in a display region.

Accordingly, Applicants respectfully assert that the rejection of claim 11 under 35 U.S.C. § 102(b) should be withdrawn because Mitanaga fails to teach or suggest each feature of independent claim 11.

Regarding the rejection of independent claim 12, it is noted that claim 12 recites a display device with a polysilicon substrate comprising: a display region; a driving region; a plurality of thin film transistors formed in the display and in the driving regions; primary and secondary crystal grain boundaries formed in the polysilicon substrate in the display region and in the driving regions; wherein the **primary crystal grain boundaries** formed **in** the **display region** are **inclined to a direction of current flowing from source to drain at an angle of -30° to 30°** and the secondary crystal grain boundaries formed in the display region are substantially perpendicular to the current flowing from the source to the drain; and wherein the primary crystal grain boundaries formed in the driving region are inclined to a direction of current flowing from source to drain at an angle of 30° to 150° and the secondary crystal grain boundaries formed in the driving region are substantially parallel to the current flowing from the source to the drain.

As noted above, Mitanaga discloses that the primary crystal grain boundaries are formed in a direction which is perpendicular to the direction of the current flowing from the source to the drain.

Contrary to Mitanaga, the primary crystal grain boundaries recited in independent claim 12, are substantially parallel to the direction of the current flowing from the source to the drain.

Accordingly, Applicants respectfully assert that the rejection of claim 12 under 35 U.S.C. § 102(b) should be withdrawn because Mitanaga fails to teach or suggest each feature of

independent claim 12.

REJECTIONS UNDER 35 U.S.C. §103:

Claims 1-5, 7, 8, 11 and 12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Mitanaga et al. (U.S. Patent 5,923,997) and further in view of Iwasaki (U.S. Patent 5,759,879).

Applicants respectfully traverse this rejection for at least the following reasons.

Regarding the rejection of independent claim 1, it is noted that Mitanaga, fails to teach or suggest each feature of independent claim 1.

Iwasaki discloses a method for forming a thin-film transistor, wherein the number of grain boundaries which intersect a current path formed in the polycrystalline silicon film is decreased and the positions of the grain boundaries are controlled (column 1, lines 29-45). Therefore, Iwasaki discloses a method for forming a thin-film transistor wherein the number of grain boundaries is reduced and the positions of the grain boundaries are controlled. Accordingly, Iwasaki is not concerned nor does it teach or suggest the location and inclination of the different types of grain boundaries in the display and driving regions of the display device, as recited in independent claim 1. Therefore, Iwasaki fails to cure the deficiencies of Mitanaga.

Accordingly, Applicants respectfully assert that the rejection of claim 1 under 35 U.S.C. §103(a) should be withdrawn because neither Mitanaga nor Iwasaki, whether taken singly or combined, teach or suggest each feature of independent claim 1.

Furthermore, Applicants respectfully assert that dependent claims 2, 4, 5 and 7 are allowable at least because of their dependence from claim 1, and because they include additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claims 2, 4, 5 and 7 also distinguish over the prior art.

Regarding the rejection of dependent claims 3 and 8, it is noted that these claims have been cancelled without prejudice or disclaimer. Accordingly, the rejection of claims 3 and 8 is moot.

Regarding the rejection of independent claims 11 and 12, as noted above, Mitanaga fails to teach or suggest the features of the independent claims.

As noted above, Iwasaki simply discloses a method for forming a thin-film transistor

wherein the number of grain boundaries is reduced and the positions of the grain boundaries are controlled. Therefore, Iwasaki is not concerned nor does it teach or suggest the location and inclination of the different types of grain boundaries in the display and driving regions of the display device, as recited in independent claims 11 and 12 and thus fails to cure the deficiencies of Mitanaga.

Accordingly, Applicants respectfully assert that the rejection of claims 11 and 12 under 35 U.S.C. §103(a) should be withdrawn because neither Mitanaga nor Iwasaki, whether taken singly or combined, teach or suggest each feature of independent claims 11 and 12.

CONCLUSION:

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 503333.

Respectfully submitted,

STEIN, MCEWEN & BUI, LLP

Date: 6/14/07

By: Douglas Rodriguez
Douglas X. Rodriguez
Registration No. 47,269

1400 Eye St., N.W.
Suite 300
Washington, D.C. 20005
Telephone: (202) 216-9505
Facsimile: (202) 216-9510